

Amendments to the Specification:

Please amend the paragraph beginning at page 3, line 8, as follows:

Figure 3 depicts a high-level block diagram of one embodiment of such a computer graphics system 50. The system 50 includes a central processing unit (CPU) 52, a display 54, a user interface 56 such as a keyboard or mouse or other communicating device, a memory 58, and an image generating unit 60 coupled with one or more buses 58. The display 54 includes a display, such as the display 1. The display [[14]] 1 also includes a display memory 55 to which data for pixels are written prior to being shown on the display 1. In order to display graphical images, the objects are broken into polygons to be used in rendering the objects. In a preferred embodiment, the polygons are rendered in raster order. That is, portions of the polygons are rendered pixel by pixel in the order of the pixels in the display 54.

Please amend the paragraph beginning at page 13, line 8, as follows:

For an example of how the method 140 functions, refer to Figures 5A-5C. For clarity, it is presumed that there are only three processors in the block of processors 64, depicted in Figure 2. Thus, the overflow parameter is three. Figure 5B depicts one way in which the display 150 can be divided into sections when the method 140 is used. The display 150 corresponds to the display 1 and, therefore, includes primitives 2, 3, 4, 5, and 6. Figure 5C depicts the bins 161-166 provided and combined by one preferred embodiment of the method 140. Preferably, the bins 161-166 are preferably of the same size. Thus, the sections 151-156 to which the bins 161-166 correspond are preferably of the same size. The display 150 is thus broken into sections 151, 152, 153, 154, 155, and 156 of equal size. Each section 151, 152, 153, 154, 155, and 156 corresponds to a particular bin 161, 162, 163, 164, 165, and 166, respectively. The primitives 2, 3, 4, 5, and 6 are stored in the bins 161-166 which correspond to the sections 161-166 that the primitives 2, 3, 4, 5, and 6 intersect. Furthermore, the primitives are stored in minimum y-value order. For example, the bin 163 includes primitive 4, [[6,]] 2, 5, and 3, in that order. It is determined whether any of the bins 161-166 can be combined without causing an overflow. Suppose three processors are available. Thus, a bin 161-166 can be combined with another bin 161-166 if the combination has three or fewer primitives 2, 3, 4, 5, and 6. If section 151 and 152

are combined, there are only two primitives 2 and 3 present in the combined section. Similarly, if sections 154, 155, and 156 are combined, there will be three primitives 4, 5, and 6 present in the combined section. As a result, bins 161 and 162 and bins 164, 165, and 166 can be combined without violating the overflow parameter. It will thus be determined in step 144 that bins 161 and 162 and bins 164, 165, and 166 can be combined. Consequently, the bins 161 and 162 are combined to form bin the 167 and the bins 164-166 are combined to provide the bin 168, using step 146. Note that the bin 163 includes four primitives, 2, 3, 4, and 5. Consequently, bin 163 will cause the system to overflow even if it is not combined. In a preferred embodiment, bins 163 will be treated separately, for example by splitting or overlaying portions of the bin 163 to be rendered separately. At least the bins 167, 163, and 168 are thus the variable-sized bins provided for rendering.

Please amend the paragraph beginning at page 16, line 14, as follows:

To further explicate the method 170, refer to Figures 6B and 5C. Figure 6B is a diagram depicting how bins are combined. Figure [[5C]] 5B depicts the sections 151, 152, 153, 154, 155, and 156 corresponding to the bins. The primitives 2, 3, 4, ~~and 5~~ and 6 are stored in the bins 161', 162', 163', 164', 165', and 166'. The bins 161', 162', 163', 164', 165', and 166' correspond to the sections 151, 152, 153, 154, 155, and 156, respectively. Because the primitives 2 and 3 cross the right boundary of the bin 161' (the section 151), the primitives 2 and 3 are stored in the right bucket 182 of the bin 161'. Because there are no primitives in the display 150 that intersect bin 161' (the section [[1521]] 151) but do not cross the right boundary of the bin 161' (the section 151), the left bucket 181 of the bin 161' is empty. Because the primitives 2 and 3 cross the right boundary of the bin 162' (the section 152), the primitives 2 and 3 are stored in the right bucket 184 of the bin 162'. Because there are no primitives that intersect bin 162' (the section 152) but do not cross the right boundary of the bin 162' (the section 152), the left bucket 183 of the bin 162' is empty. Because the primitives 4 and 5 cross the right boundary of the bin 163' (the section 153), the primitives 4 and 5 are stored in the right bucket 186 of the bin 163'. Because the primitives 2 and 3 intersect bin 163' (the section 153) but do not cross the right boundary of the bin 163' (the section 153), primitives 2 and 3 are stored in the left bucket 185 of the bin 163'.

Because the primitives 4 and 5 cross the right boundary of the bin 164' (the section 154), the primitives 4 and 5 are stored in the right bucket 188 of the bin 164'. Because there are no primitives that intersect bin 164' (the section 154) but do not cross the right boundary of the bin 164' (the section 154), the left bucket 187 of the bin 164' is empty. Because the primitive 6 crosses the right boundary of the bin 165' (the section 155), the primitive 6 is stored in the right bucket 190 of the bin 165'. Because the primitives 4 and 5 intersect bin 165' (the section 155) but do not cross the right boundary of the bin 165' (the section 155), primitives 4 and 5 are stored in the left bucket 189 of the bin 165'. Because no primitives cross the right boundary of the bin 166' (the section 156), the right bucket 192 of the bin 166' is empty. Because the primitive 6 intersects bin 166' (the section 156) but does not cross the right boundary of the bin 166' (the section 156), the primitive 6 is stored in the left bucket 181 of the bin 162'.